Simulation and Analysis of DDR3 Bus Based on Fly-By Topology with Cadence

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Abstract. For the requirements of different bus signals from high speed PCB with DDR3 components based on fly-by topology structure, coping strategies have been proposed respectively. For the address or command bus, a leveling-free strategy has been proposed. It shows that the phase difference can be nearly zero through reasonable constraints on PCB design. The strategy was applied to the clock bus and achieved good performance, combining with the rules of signal integrity. For the data bus, the timing sequence on source synchronous has been analyzed and the time margin was calculated. The reasonability of the design was verified through the simulation result with Cadence.

Introduction

Along with the development of electronic design and chip manufacturing technology, more challenges are brought to PCB designers, especially for high speed PCB design. As popular memory chip, DDR3 SDRAM has been widely applied to the occasions where need high speed memory. The DDR3 interface for a data rate of 1600MHz or even higher typical for consumer electronics products was implemented [1]. The DDR3 interface circuit for this paper comes from one data acquisition card of the current project. The design has used DDR3 memory module, for large amounts of data require being stored in the data acquisition process. Analysis on the timing sequence and simulation tests must be done before PCB layout to ensure the timing requirements.

The design structure of data acquisition system

Timing analysis and simulation of DDR3 module of the DAQ board based on FPGA and PCI-e bus interface has been done in this paper. The structure of the DAQ system is shown in Fig.1. As there is difference between the data sampling end and the sending end, DDR3 memory module has been designed to guarantee against data loss. The sampling data will be stored after processing, waiting the host to read through PCI-e interface.

Fig.1  The design diagram of DAQ system
Induction about DDR3 principle

For the data bus, DDR3 SDRAM has applied the ODT technology, so there is no need to connect termination resistor. While for others, note that the DDR3 chip set adopts fly-by topology structure, which is very different from T connection structure applied by DDR2. Fig.2 shows the two kinds of structure.

![Fig.2](image)

T structure requires the distances between all memory components and the T point to be equal to guarantee the same flight time. It brings too much nodes and signal noise, though it can be easy to control the timing sequence. Therefore DDR3 adopts fly-by topology structure, which is a special case of a daisy chain with a very short or no stub [2]. It improved the signal integrity through reducing the branches and implemented point-to-point connection. However, for the own fly-by structure of DDR3, extra skew of flight time is brought in to fly-by signals [3]. The DDR3 fly-by topology requirement means customers designing DDR3 memories must now account for write leveling and read deskew on the PCB [4].

Note that for the common FPGA components such as Cyclone and Arria series, there’s no available leveling circuit in the chips, though DDR3 memory is supported. One thought is adjusting the phases by taking advantage of signal reflection to reduce the phase difference between the DDR3 components. On the other hand, the timing constraints on DDR3 memory interface have important influence on data access. DDR3 adopts the source synchronous technology, thus accurate analysis about the timing sequence and constraints on layout must be done before PCB design [5], in order to ensure the design meeting the requirements of setup and hold time [6].

Simulation and analysis

Simulations on address bus. The fly-by routing follows the rules that starting at the controller then connecting to the lowest data bit chip first and ending at the highest data bit chip [7]. The topology structure is shown by Fig.3. P1 is the controller component. U9 and U10 are respectively the high and low bit chips of memory. RN3 is the termination resistor. Actually the stub between components and fanout vias can be removed, which means the dills can be placed on the pins directly, thus make the stub in fly-by structure tend to be 0 (just like the pin of P1 in the picture). Therefore, lines need to be adjusted are mainly L1, L2 and L3, which are defined in Table 1.

![Fig.3](image)

Secondly, make sure the suitable position of RN3. It has important effect on signal integrity, though there is no difference on electrical connection whether the termination resistor is located in the middle or at the end. Change the position of RN3 after giving IBIS models to the I/O pins of P1, U9 and U10. The results are shown in Fig4 and Fig5. Table 1 also shows the length value (unit: mil).
Comparing the above results, it is not difficult to find that:
When RN3 is located at the middle of the fly-by structure, the back reflection of the signal has significant interference on the sending end, which brings the high level of the sending end an obvious trough. While the forward reflection produces a phase correction to the received waveform of U9 in the downstream, compensating the phase difference between the two memory chips. An intersection close to the high or low threshold on the rise and fall edges can be found from the waveforms of U9 and U10. We can just call it phase compensation point. While RN3 is located at the end of the fly-by structure, though the interference on the sending end from the back reflection is weakened and the waveform tends to be smoother, there is always a certain phase difference between the two receiver chips. It can be seen that the difference is about 0.14ns, which can never be ignored in timing sequence design of DDR3.
So in the premise of not destroying the monotonicity of the source signal, it’s better to choose the termination located in the middle position. Thus we can make the phase difference of fly-by signals close to 0 by appropriately adjusting the routing constraints of PCB design. While the larger interference to the sending end caused by the back reflection can be further weakened by adjust the size of the termination resistor. Select the termination resistor respectively to be 51ohm and 39ohm. It can be found that the trough on the high level of the sending end was elevated by 35mv compared to the former. After determined the location and size of the termination resistor, adjust the line length to obtain the desired results. As is shown in Fig.6, the signal phase of U10 and U9 has a perfect matching. The simulation parameters are shown in Table 2(unit: mil).

### Table 1  The address lines definition in section

<table>
<thead>
<tr>
<th>Line</th>
<th>From</th>
<th>To</th>
<th>Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>L0</td>
<td>Pin</td>
<td>Via</td>
<td>20</td>
</tr>
<tr>
<td>L1</td>
<td>P1</td>
<td>U10</td>
<td>1800</td>
</tr>
<tr>
<td>L2</td>
<td>U10</td>
<td>U9</td>
<td>500</td>
</tr>
<tr>
<td>L3</td>
<td>U10</td>
<td>RN3</td>
<td>200</td>
</tr>
</tbody>
</table>

Fig.4  RN3 located at the middle

Fig.5  RN3 located at the end

Furthermore, the simulation made a attempt by increasing the number of DDR3 SDRAM chips. Fig.7 is the simulation results when increasing the number to 3. As is shown, the received waveforms are

### Table 2  The address lines parameter list

<table>
<thead>
<tr>
<th></th>
<th>L0</th>
<th>L1</th>
<th>L2</th>
<th>L3</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>20</td>
<td>1600</td>
<td>650</td>
<td>200</td>
</tr>
</tbody>
</table>

Fig.6  The final result after adjustment

Fig.7  The situation with 3 memory chips
well matched. It should be mentioned that the termination resistor should be always in the front of the fly-by structure. And with increasing the number of chips, the length of $L_1$, which is from the controller to the first memory chip, need to be extended (The length of $L_1$ is 2300mil in the picture). Notably, the line’s layer distribution has influence on the phase compensation point. This should be related with the different transmission speed of the surface layer and the inner. According to the two models of transmission line, the speed for the surface layer is about 143ps/inch while the latter is 180ps/inch, which respectively means 6.98 inch/ns and 5.5 inch/ns [8].

In addition, the effect of vias should be considered as well. For the signal reflection, a via will increase the jitter and narrow eye width, resulting in data misreading of the receiver [9]. For the timing sequence, the via can cause extra delay. For instance, a via with 10 mil diameter dill can cause a 23ps delay [10].

Simulation results also proved the point. For example, if add fanout via to the pin and distribute the line in the inner layer, the length of $L_1$ should be about 1600mil. While laying directly on the surface, other parameters unchanged, the length requires being prolonged to 1800mil. Certainly, different situations need to be determined by practical simulation.

**Simulations on differential pair of clock bus.** For the DDR3 interface circuit of FPGA, the clock bus is not only fly-by signal, but also in differential form. For the differential pairs, not only the length, the relative delay and line spacing need to be considered as well. The differential pairs of DDR3 interface circuit include clock signal and data strobe signal. The clock signal is not only in differential form, but also has fly-by topology structure which is shown in Fig.8.

Due to the unique structure of the clock signal, the wiring rules about both differential pair and fly-by structure need to be considered. First set differential line spacing with the constraint manager, and then determine the length by the simulation results of fly-by topology, finally adjust the length difference of the differential pair to determine the relative delay. Constraint rules eventually ascertained are shown in Table 3. The width of the differential lines is 4mil, line spacing is 5mil. The simulation results are shown in Fig.9.

**Table 3 The constraint rules on clock lines**

<table>
<thead>
<tr>
<th>Line</th>
<th>From</th>
<th>To</th>
<th>Length[mil]</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1</td>
<td>P1</td>
<td>U10</td>
<td>1700–1710</td>
</tr>
<tr>
<td>L2</td>
<td>U10</td>
<td>U9</td>
<td>650–660</td>
</tr>
<tr>
<td>L3</td>
<td>U10</td>
<td>R90</td>
<td>50</td>
</tr>
</tbody>
</table>

![Fig.8 The topology structure of differential clock bus](image)

![Fig.9 The simulation waves of clock bus](image)
It can be seen that the clock signals’ relative delay of the two memory chips caused by the fly-by structure is only around 36ps, while the single memory chip’s phase error of the differential clock signals caused by line deviation is about 79ps, which respectively accounted for 1.4% and 3.2% of one clock cycle. In addition, it should be mentioned that the value of termination resistor (R90 in Fig.9) must be suitable. If not, the signal’s back reflection will seriously affect the quality of source signals, while the forward reflection will bring additional clear overshoot on the downstream chip (U9 in Fig.9). Thus different termination resistor values need to be tested to determine the right one.

**Simulations on data bus.** The read-write principle of external memory interface of Cyclone V series FPGA is shown in Fig.10 [11].

![Fig.10 The read-write schematic diagram of external memory interface for Cyclone V series](image)

It can be seen that the read and write process use source synchronous signal DQS as read and write clock signal. The ideal relation is the flip edge of the source synchronous clock signal always in the central position of the data signal, thus can ensure maximum setup and hold time margin. As the output signals provided by the controller itself meet this performance, therefore only need to ensure that the two signals’ flight times are completely consistent.

For writing operation, if regard the output moment of the pin buffer at the sending end as the reference start point, the setup and hold time margin equations can be obtained as Eq.1 and Eq.2 [12]. $T_{vy}$ is the time that the data is still valid after the strobe at the beginning of output from the drive end, and $T_{vb}$ as the data’s valid time before the strobe. The skew is defined by Eq.3.

\[
T_{\text{setup\_margin}} = T_{vb} - T_{\text{setup}} + T_{\text{pcb\_skew}} \tag{1}
\]

\[
T_{\text{hold\_margin}} = T_{vy} - T_{\text{hold}} - T_{\text{pcb\_skew}} \tag{2}
\]

\[
T_{\text{pcb\_skew}} = T_{\text{flt\_strobe}} - T_{\text{flt\_data}} \tag{3}
\]

Select the clock frequency as 400MHz, and the setup and hold time can be checked out by DDR3 datasheet, then $T_{\text{setup}} = 125\, \text{ps}, T_{\text{hold}} = 150\, \text{ps}$. $T_{vy}$ and $T_{vb}$ depend on the output of FPGA component. For writing process, $T_{vb} = T_{vy} = \frac{1}{4}T_{\text{clk}} = 0.625\, \text{ns}$. Let $T_{\text{setup\_margin}} \geq 0$ and $T_{\text{hold\_margin}} \geq 0$, then feed the values into the two equations above, we can have $-0.5\, \text{ns} \leq T_{\text{pcb\_skew}} \leq 0.475\, \text{ns}$.

In addition, as the logic level of the data signal has dual threshold, it actually defines the maximum and minimum flight time. $T_{\text{flt\_min}}$ is defined as the flight time from the buffer outputs signal at the sending end to the rising edge reaches the low level threshold $U_{il}$ at the receiving end, while $T_{\text{flt\_max}}$ corresponding the high level threshold $U_{ih}$. Therefore, Eq.6 has changed to be Eq.4.

\[
T_{\text{pcb\_skew}} = T_{\text{flt\_strobe\_min}} - T_{\text{flt\_data\_max}} \tag{4}
\]

To be clear, DDR3 chips use two pairs of threshold value for the data signal, the AC values and the DC values. In general situations, the AC thresholds are $\pm 150\, \text{mV}$ than the reference voltage, and the DC thresholds are $\pm 100\, \text{mV}$ than the reference voltage. The AC thresholds actually define the start
time of logic level and the DC thresholds define the end time. Therefore, the referenced thresholds of
the above theoretical analysis of flight time are actually the AC values. While the two related
parameters provided in the simulation tool of Cadence are $T_{\text{SettleDelay}}$ and $T_{\text{SwitchDelay}}$, the delay time
respectively for settling and switching, and the referenced thresholds are DC values. Under the
condition that the signal ringbacks do not exceed DC thresholds, it will meet that $T_{\text{SettleDelay}} < T_{\text{fb max}}$, $T_{\text{SwitchDelay}} > T_{\text{fb min}}$, and their difference can be measured by the simulation results. The values are
about $\Delta T_1 = 20\,\text{ps}$, $\Delta T_2 = 50\,\text{ps}$. In the theoretical calculation the effect of $\Delta T_1$ and $\Delta T_2$ can be
ignored, taken as the design margin, further to ensure the reliability of the design. Therefore the actual
skew time can be calculated by Eq.5.

$$T_{\text{pcb skew}} = T_{\text{strobe SwitchDelay}} - T_{\text{data SettleDelay}}$$

(5)

Through the reflection simulation it showed that the data line length was about 1250mil when there’s
a good signal quality. Therefore the length constraint can be 1245mil~1265mil. The extreme values
were tested respectively. The simulation results are shown in Table 4.

Table 4  The simulation results of data bus on writing

<table>
<thead>
<tr>
<th>Length</th>
<th>1245[mil]</th>
<th>1265[mil]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DQ</td>
<td>DQS</td>
</tr>
<tr>
<td>Switch Delay[ns]</td>
<td>0.93749</td>
<td>1.23042</td>
</tr>
<tr>
<td>Settle Delay[ns]</td>
<td>1.04941</td>
<td>1.38435</td>
</tr>
</tbody>
</table>

Therefore, $T_{\text{pcb skew}} = 1.23042 - 1.07345 = 0.15697\,\text{ns}$.

For reading process, the strobe signal comes from the memory would first suffer a phase-shift of 90
degrees through the DLL module within FPGA, and then serve as clock signal to the input register.
Therefore, slightly different from the write operation, calculation formulas of read operation are
shown by Eq.6 and Eq.7.

$$T_{\text{setup margin}} = T_{\text{vb}} + \frac{1}{2} T_{\text{clk}} - T_{\text{setup}} + T_{\text{p pcb skew}}$$

(6)

$$T_{\text{hold margin}} = T_{\text{va}} - \frac{1}{2} T_{\text{clk}} - T_{\text{hold}} - T_{\text{p pcb skew}}$$

(7)

From the datasheets, $T_{\text{setup}} = -0.819\,\text{ns}$, $T_{\text{hold}} = 0.972\,\text{ns}$, $T_{\text{vb}} = -0.2\,\text{ns}$, $T_{\text{va}} = 0.95\,\text{ns}$. Note that the
value of $T_{\text{setup}}$ and $T_{\text{vb}}$ are negative, which means that the data is valid after the strobe signal.
Let $T_{\text{setup margin}} \geq 0$, $T_{\text{hold margin}} \geq 0$, and feed the values into the two equations above, we can have the
result that $-0.619\,\text{ns} \leq T_{\text{p pcb skew}} \leq 0.478\,\text{ns}$. The simulation result is shown in Table 5.

Table 5  The simulation results of data bus on reading

<table>
<thead>
<tr>
<th>Length</th>
<th>1245[mil]</th>
<th>1265[mil]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DQ</td>
<td>DQS</td>
</tr>
<tr>
<td>Switch Delay[ns]</td>
<td>0.51102</td>
<td>0.56550</td>
</tr>
<tr>
<td>Settle Delay[ns]</td>
<td>0.63008</td>
<td>0.68872</td>
</tr>
</tbody>
</table>

Thus it can be calculated that $T_{\text{p pcb skew}} = 0.56550 - 0.63306 = -0.0676\,\text{ns}$.

It can be seen that the reading and writing skew time calculated according to the simulation results
completely met the source synchronous timing requirements. The results represent the total flight
time deviation, including not only the skew caused by PCB routing, but also the delay difference of
the inner I/O buffer of the component. In practice, there is also the clock jitter interference. Therefore,
fully consideration must be taken on PCB design, leaving allowance to these factors.
Conclusions
Under certain conditions, for the address/command/control bus, through rational use of termination resistor and electronic circuit design, the phase delay brought by the fly-by structure can be greatly reduced and even close to 0. For the clock bus, requirements of both the fly-by structure and signal integrity need to be considered comprehensively, in order to obtain better waveform. For the data bus, modeling on timing sequence and theoretical calculations have been done to ensure that the design meets the source synchronous timing requirements. Combining with the parameters provided by the simulation tool of Cadence, the source synchronous timing margin of the design can be obtained through the analysis and derivation of the source synchronous timing, providing a theoretical basis for the design. These design schemes allow us to use some medium to low-end chips that do not support signal leveling to design DDR3 memory interface based on fly-by structure, so as to obtain a faster speed and larger capacity. This can have high practical value in application.

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