Research of Low Power Design Strategy Based on IEEE 1801 Unified Power Format

ShuPing Cui\(^1,\)\(^a\), Chuang, Xie\(^1,\)\(^b\)

\(^1\)Lab of Industrial Control Network and System Shenyang Institute of Automation, Chinese Academy of Sciences, Liaoning Shenyang, China
\(^a\)cuisp@sia.cn, \(^b\)xiechuang@sia.cn

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Abstract. Power consumption is becoming an increasingly important aspect of circuit design. High power consumption can lead to high machine temperature, short battery life which makes laptop electronics difficult to be widely used. IEEE 1801 Unified Power Format (UPF) is designed to express power intent for electronic systems and components. This paper first introduces the power principles, puts forward the approaches to reduce power consumption according to UPF, and then demonstrates the Synopsys design flow based on UPF, finally gives the power report and makes a conclusion.

Introduction

In recent years, the device densities and clock frequencies have been higher and higher, at the same time, the supply voltages and transistor threshold voltages have been lowered in CMOS devices, so power consumption has been dramatically increased. Increased power consumption can lead to a series of headache problems such as high machine temperature which makes users uncomfortable and requires expensive cooling systems, low battery life which restrict the widely use of laptop electronics. For millions of computers, servers, and other electronic devices used on a large scale, even a little rise of power consumption can cause enormous electrical energy waste. At the same time, even a small reduction in power consumption can result in large aggregate cost savings and can provide significant benefits to the environment as well\(^{[1]}\).

The Unified Power Format (UPF) is a standard set of Tcl-like commands used to specify the low-power design intent for electronic systems. The official Unified Power Format, version 1.0, was approved in February 2007 by Accellera. Accellera is an electronics industry organization focused on creating electronic design automation standards that can be used throughout the industry. Accellera transferred the UPF copyright to the IEEE P1801 Working Group for further expansion and refinement of the power specification standards and for formal approval as an IEEE standard. IEEE 1801™-2013 ", the newest revised version, was announced at 30 May 2013 \(^{[2]}\).

1. The types of power

There are two types power that we must consider during chip operation, dynamic and static power.

1.1. Dynamic power

Dynamic power is the energy consumed during logic transitions on nets, consisting of two components, switching power and internal power.

Switching power results from the charging and discharging of the external capacitive load on the output of a cell. Switching power consumption depends on the clock frequency (possible transitions per second) and the switching activity (presence or absence of transitions actually occurring on the net in successive clock cycles).

Internal power results from the short-circuit current that flows through the PMOS-NMOS stack during a transition. When the input signal is at an intermediate voltage level, the PMOS and NMOS transistors can be conducting both. This condition results in a nearly short-circuit conductive path.
from VSS to ground. Lower threshold voltages and slower transitions result in more internal power consumption.

1.2. Static power
Static power is also called leakage power which is caused by leakage current including reverse-bias p-n junction diode leakage, subthreshold leakage, and gate leakage. Leakage power is becoming increasingly significant with shrinking device geometries and reduced threshold voltages. Leakage currents occur whenever power is applied to the transistor, irrespective of the clock speed or switching activity. Leakage cannot be reduced by slowing or stopping the clock.

However, it can be reduced or eliminated by lowering the supply voltage or by switching off the power to the transistors entirely.

2. Low power design strategy
There are many kinds of ways to reduce power, such as clock gating, dynamic voltage, and frequency scaling etc. And most of these strategies can be implemented using UPF commands.

2.1. Clock gating and power switching
Clock gating has been used widely and successfully for a long time. In some circumstance registers need to maintain the same logic values over many clock cycles. Reloading the registers with the same value on each clock cycle causes power waste. If the clock is gated, the power will be reduced. According to the design, clock gating can be inserted intently during RTL design. Synthesis tool for example design compiler (DC) can also find low-throughput data paths and automatically done this work. This kind of work can be checked from the command log file.

Power switching is different from clock gating because parts of the chip are shut down completely during periods of inactivity by cutting the supply voltage which is called power down mode. Before they are in use, they must be “wake up”. In power down mode, there is no leakage and switching power, which can dramatically reduce power consumption. The implementation of power switching needs the help of a power controller, a power-switching network, isolation cells, and retention registers. A power controller is a logic block that determines when to power down and power up a specific block. The network connects the power to or disconnected the power from the logic gates in the block. Isolation cells are used to connect power on module and power down module. When both modules are on, they like wires. When one is off, they can provide a known, constant logic value to an always-on block. Before power down, the value of registers should be saved and restored after power on by retention register. The relevant commands of UPF are create_power_switch, map_power_switch, set_isolation, and set_retention etc.

2.2. Dealing with voltage
Supply voltage reduction can reduce power effectively. According to the formula Power = IV = V^2/R, A 50 percent reduction in the supply voltage results in a 75 percent reduction in power. But lower voltage can cause low speed and some other problems, such as, noise immunity, crowbar currents, and sub-threshold leakage. Of course, different parts in a chip might have different speed. So multivoltage can be implemented to save power. Even the voltage can be changed dynamically according the operating status. So is the clock’s frequency. The relevant commands of UPF are create_power_domain, create_supply_net, create_supply_port, set_domain_supply_net, and so on.

2.3. Using Multiple-Vt Library Cells
Some CMOS technologies support the fabrication of transistors with different threshold. The cells have the same logic function but different transistor threshold. Low-Vt leads to higher speed, and higher sub-threshold leakage current. High-Vt leads to low leakage current, but less speed. Synthesis’ tool can decide which cell to use. When timing is critical, low-Vt cells are used. When timing is loose, High-Vt cells are chosen. High-Vt transistors are used as power switches and retention register because they minimize leakage and their switching speed is not critical.
3. The Synopsys low power flow

The Synopsys low-power flow is shown in Figure1. First Design Compiler reads in the RTL and UPF1 files, and synthesizes a gate-level net list and a UPF2 file. The DC commands are Load_upf and save_upf. Then IC Compiler reads in the gate-level net list and the UPF2 file, after physical implementation produces a modified gate-level net list, a complete power and ground (PG) netlist, and an updated UPF file. VCS and MVSIM can be used for functional verification of the multivoltage design. MVRC checks for adherence to multivoltage rules and reports any problems related to power. PrimeRail performs voltage drop and electro migration analysis for gate-level and transistor-level designs. PrimeTime does timing analysis with UPF information.

![Synopsys low-power flow diagram](https://example.com/synopsys_diagram.png)

Figure1 Synopsys low-power flow

4. Report analysis

TSMC is the world’s largest dedicated semiconductor foundry. It supplies 180nm CE018FG ULL (ultra low leakage) technology library to support ultra low power design. Synthesis base on UPF using ULL (ultra low leakage) technology library and normal flow using base technology library are done respectively, and two different power reports are got. The contrast between them is shown in table1.

<table>
<thead>
<tr>
<th>category</th>
<th>ULL flow</th>
<th>Normal flow</th>
</tr>
</thead>
<tbody>
<tr>
<td>total static power</td>
<td>4.4750 mW</td>
<td>6.5583 mW</td>
</tr>
<tr>
<td>dynamic power</td>
<td>8.1424 mW</td>
<td>12.2461 mW</td>
</tr>
<tr>
<td>cell internal power</td>
<td>3.6673 mW</td>
<td>5.6879 mW</td>
</tr>
<tr>
<td>net switching power</td>
<td>1.9220 uW</td>
<td>13.2836 uW</td>
</tr>
</tbody>
</table>

From the data of table, both the static and dynamic power is reduced. DC is not expert power analyzer. Comprehensive power analysis should be performed by Primetime PX after physical implementation.

5. Conclusions

With the improvement of science, plenty of electric devices consume enormous energy. Energy consumption causes the worse environment on the earth. Reduction power consumption becomes extremely urgent. Low power strategy base on IEEE 1801 Unified Power Format can reduce power consumption of chips dramatically. With the wide application of this technology, the problems will be solved finally.
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