The Design and implement for Transceiver of WIA-PA

Duan Maoqiang\textsuperscript{1, a}, Huang Xiaoli\textsuperscript{2, b} and Wang Jianjun\textsuperscript{1, c}

\textsuperscript{1}Lab. of Networked Control System, Shenyang institute of Automation, Chinese Academy of Sciences, Liaoning Shenyang, China
\textsuperscript{2}Competitive Intelligence Center Institute of Scientific & Technical Information of Liaoning Province, Liaoning Shenyang, China
\textsuperscript{a}duanmaoqiang@sia.cn, \textsuperscript{b}sophieya@yeah.net, \textsuperscript{c}wangjj@sia.cn

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Abstract. In this paper, the system scheme and system architecture for transceiver of WIA-PA are presented. The low-IF topology and direct up conversion method are employed, corresponding to receiver part and transmitter part. And in the baseband part, differential and correlation demodulate received signals, as well as time sync, frequency offset calibrate and frame sync operations are designed for solvation the problem of real radio environmental effects. The chip implements using 0.18\textmu m CMOS process has small chip area and low power consumption. The minimum sensitivity of receiver is less than -85dBm for 1\% PER (packet error rate), which is better than the required sensitivity for specification.

Introduction

Wireless communication technologies are successfully introduced in industrial fieldbus, due to the character of low cost in this century. But, it also has some issues hardly to overcome, such as harsh industrial field environments such as low power, high reliability, real-time. Fortunately, WIA-PA (Wireless Networks for Industrial Automation - Process Automation) is of important role in industrial wireless technology for providing a self-organizing, self-healing smart mesh network routing mechanism, and high reliability, strong stability, real-time network performance, and the independent intellectual property right of which has been possessed in China. WIA-PA network is always used in industrial monitoring, measurement and control applications, typically applied in wireless sensor network for remotely monitoring and accessing much key parameters of industrial process, aims to optimal control, improving work effectively and implementing power saving. And now it has become one of the three documents of international standardization together with wireless Hart and ISA-100.

Nowadays, much researches have been focused on WIA-PA [1][2][3]. Ref 1 pay attentions to time synchronization of WIA-PA, which takes away building the logic synchronization tree to improve the precision of multi-hop FTSP clock synchronization. Then it use precision Bayesian estimation to improve the accuracy of clock synchronization. Ref. 2 proposed adaptive channel hopping scheme by considering the interference characteristic. Ref. 3 used a method of cross-layer design to solve the problem of less real-time reliable communication in tradition OSI seven layer network architecture.

WIA-PA network protocol following reduced ISO/OSI seven layer network architectures, only defines the physical layer, data link layer, network layer and application layer. The PHY layer of WIA-PA is compliance with IEEE 802.15.4 standard protocol. Our work is focused on WIA-PA physical layer design and implement. The remainder of this paper is the following: In section 2, we review the key parameters of IEEE 802.15.4 for physical layer and a system scheme will be present. Meanwhile, detail architecture design and conclusion would be described in section 3 and section 4, respectively.

System parameters and scheme

IEEE 802.15.4 protocol operates in three license-free bands: 2.45 GHz, 868 MHz for North American; 915 MHz for Europe. WIA-PA’s physical layer operates in 2.45 GHz too.
HS-OQPSK (half sine offset-quadrature phase shift keying) modulation is employed. And support over-the-air data rate of 250Kbps [4]. Details parameters are listed:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency band</td>
<td>2400MHz~2483.5MHz</td>
</tr>
<tr>
<td>Modulate scheme</td>
<td>DSSS</td>
</tr>
<tr>
<td>Symbol rate</td>
<td>62.5Kbps</td>
</tr>
<tr>
<td>Channel spacing</td>
<td>5MHz</td>
</tr>
<tr>
<td>Adjacent channel rejection</td>
<td>0dB</td>
</tr>
<tr>
<td>Total channel number</td>
<td>16</td>
</tr>
<tr>
<td>Receiver sensitivity</td>
<td>Better -85dBm</td>
</tr>
<tr>
<td>Frequency deviate tolerate</td>
<td>±40 ppm</td>
</tr>
</tbody>
</table>

The physical layer employs a 16-ary quasi-orthogonal modulation technology. During each data symbol period, four bits information are used to map by 16 orthogonal pseudo-random noise sequences to be transmitted. The transceiver of PHY is needed to have a capability of achieving sensitivity of -85 dBm or better, and frequency deviate tolerate of ±40 ppm. The 2 MHz chip rate generates a transmit spectrum with 2 MHz bandwidth.

It is well known that low-IF topology is suitable than the others to use in the scheme of receiver. The external filters, like off chip image rejection filters used in heterodyne receiver architecture, is also needed to suppress the additional mixing process and second LO signal in double conversion receiver architecture, but both of them suffer from higher power consumption. Well, the direct conversion is a low power selected scheme, but it has the drawback of poor immunity to DC offset noise due to the second order distortion and mismatch. And flicker noise of CMOS transistors covers the entire signal band in narrowband, which is difficult to cancel. And the major challenge of low IF topology is limited image rejection arising from the non-perfect balance of the in-phase and quadrature signal used to implement a complex valued mixing process. However, the need of 0 dB adjacent channel rejection, specification of the image rejection is not tight in the 802.15.4 standard, lead to low IF topology becomes an appropriate choice.

In the scheme of transmitter adopts a direct up conversion IQ modulation, the benefit of which is the flexibility to use simple, low cost and low power due to less linear power amplifiers in the transmit path.

**Details of system architecture**

The transceiver architecture is designed according to the protocol parameter specification and system scheme. As shown in Fig.1, the architecture is composed of three parts: Radio frequency front end, digital baseband and MAC operation. Also divided by function, both transmitter part and receiver part are included.

In transmitting data case, BTS (bit to symbol) is defined to encode all binary data contained in the PPDU (PHY protocol data unit). Each octet will map into one data symbol. Then, STC(symbol to chip) module is followed. Each data symbol will be mapped into a 32 chip PN sequence. The PN sequences are related to each other through cyclic shifts. Function of MAS (modulate and shaping) is that chip sequences are modulated using O-QPSK with half sine pulse shaping. Then, the modulated baseband digital waveform transform to analog signal using DAC (digital analog converter), and LPF (low pass filter) following DAC is needed to filter many unwanted spurious signal included to satisfy the output spectrum mask requirement. Finally, PA (power amplifier) amplifies up conversion signal, which is mixed between baseband signal and local oscillator.
In receiver data case, RF_end part consists of LNA (low noise amplifier), mixer, PLL-based quadrature frequency synthesizer, CBPF (complex band pass filter), PGA (program gain amplifier) and ADC (analog digital convor). PGA is placed in front of the ADC, adapting the loss variation of the transmission channel in order to ease the dynamic range requirement for the ADC [5]. The PGA is required to adjust the amplitude of the received signal depending on the signal level so as to keep almost constant signal level at the ADC input. AGC (auto gain control) provide a gain control scheme to PGA in digital domain from I/Q complex signal. The receiver maximum gain is 60dB [6], calculated as follows:

\[ G_{max} = \text{REF}_{ADC} - 6N_{ADC} + \delta_{ADC} + \text{SNR}_{min} + M \text{rgn-Rss} \]  

(1)

The digital low IF signals I/Q will convert to clear baseband I/Q signals using DDC (digital down frequency converter) and LPF. Followed time synchronization, frequency synchronization and frame synchronization will be operation; the corresponding components are TS (time sync), FOE (frequency offset estimate), and SFD (start delimitation of frame detector). The estimate values feedback DDC from FOE is used to calibrate the frequency offset, otherwise, demodulator is getting difficult under the severe frequency offset. The DM (demodulator) is the key of component for receiver, we will adopt scheme of differential and correlator to demodulate. The detail of mathematical derivation is followed:

Assumed \( r(k) \) is received signal, and \( s_n \) is a pulse shaped transmission signal.

\[ r(k) = s_n(k)e^{j2\pi\Delta f_k} \]  

(2)

Here, \( k \) is a time index, \( n \) is a data index, range from 0 to 15. And \( \Delta f \) is frequency offset of a carrier. Let, multiplication delay differential, the result of which expressed in Eq.3

\[ D_r(k) = r(k)r^*(k - NT_c) = s_n(k)s_n^*(k - NT_c)e^{j2\pi\Delta f NT_c} \]  

(3)

The differentiated PN sequence complex conjugate can expressed as Eq.4. And correlation calculation follows Eq.5. Here \( m \) is a data index, range from 0 to 15.

\[ D_s(k) = s_m(k)s_m^*(k - NT_c) \]  

(4)

\[ C(k) = D(k)[D_s(k)]^* = s_n(k)s_m^*(k)s_m(k - NT_c)s_n^*(k - NT_c)e^{j2\pi\Delta f NT_c} \]  

(5)
\[ |C(k)| = \begin{cases} 1, & n = m \\ < 1, & n \neq m \end{cases} \quad (6) \]

As shown in Eq. 6, the maximum value at the time \( n \) is equal to \( m \). By the way, the \( \Delta f \) has been eliminated in the previous operation, even if the value is also small. Therefore, we can get a correct demodulated transmission data.

**Conclusions**

A transceiver for WIA-PA based on the IEEE 802.15.4 standard is presented. The chip implements using 0.18\( \mu \)m CMOS process has small chip area and low power consumption. The minimum sensitivity of receiver is less than -85dBm for 1% PER (packet error rate), which is better than the required sensitivity for specification.

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**References**

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