Design of RFID Base-band Transmission Model and IP Core

Lianbo Ma¹, Kunyuan Hu¹, Ben Niu²

¹Shenyang Institute of Automation, Chinese Academy of Sciences, Shenyang 110016, P.R. China
²School of Management, Shenzhen University, Shenzhen, 518060 P.R. China
malb@sia.cn, kunyuanhu@sia.cn, drniuben@gmail.com

Abstract

This paper proposed a RFID base-band transmission model based on the analysis of RFID base-band communication course, in which FPGA technology is employed to design a communication IP core, integrating functions of base-band encoding & decoding and data transmitting. The RTL design of base-band communication IP core based on modular method is also presented. The experimental studies based on Quartus II and Simulink simulating tools indicate that the proposed communication model is fully feasible, providing a highly-integrated baseband communication IP core.

1. Introduction

A typical RFID (Radio Frequency Identification) system includes two components: electronic tags and readers. Generally, the electronic information programmed with unique format is stored in the tags. Reader which includes control unit and front-end RF unit can read electronic tags’ information by emission of radio waves in ranges which can reach up to 100 feet or more, depending on its power output and the radio frequency which is used.

The base-band part of RFID, which can connect the control unit to the front-end RF unit for the transparent transmission, is the key to ensure the reliable communication. The research of the base-band process which includes base-band encoding & decoding, verification and signal filtering, has become hot in the field of wireless communications.

In this paper, based on RFID applications and EPC protocol, using PIE-encoding and Miller-decoding technology [1], the base-band transmission model is given. And a sort of base-band IP core based on that model is designed, which has functions of high-speed encoding & decoding, internal task scheduling and data control. And the IP core and the transmission model are verified and simulated.

2. Based-Band Transmission Model of RFID System

The base-band transmission model of RFID system consists of three components: the reader’s base-band signal process, the tag’s base-band signal process and transmission channel as shown in Fig.1.

![Fig. 1 Base-band transmission model of RFID system](image)

In the downlink communication, the PIE (Pulse Interval Code) is used in the encoding course according to EPC protocol. As shown in Fig.1, Tari of PIE is the reference interval based on EPC protocol type A [2]. As one pulse of the above code can represent a number of binary symbols, it is more appropriate in high-speed transmission system [3]. A multi-band code such as PIE adopted in the RFID system is aimed to raise the information rate at a certain code rate.

![Fig. 2 PIE code](image)
In the above model, mathematical model of downlink communication can be abstracted as shown in Fig. 3.

\[
y(t) = \sum_{j=0}^{\infty} ah[(jT_s + t_0) - kT_s] + ns(jT_s + t_0).
\]

Where \( a_k \) is the \( k \)th symbol in the input symbols \( \{a_k\} \), \( h(n) \) is the characteristic function of the system’s impact response, \( y(t) \) is zero state response of \( h(n) \), \( n(t) \) is the output noise generated by additive noise \( n(t) \) through the characteristic function of the reception filter. The sampling & judging module is sampling \( y(t) \) to determine the digital information sequence \( \{a_k\} \). To judge the value of \( a_k \), \( y(t) \) is sampled at \( t = jT_s + t_0 \), \( t_0 \) is the delay of transmission.

Because of the random inter-symbol interference and noise, the random error is generated when the sampling & judging circuit is judging. For an example, supposing that the possible value of \( a_k \) is 0 or 1, and the threshold voltage of the sampling & judging circuit is \( v_0 \) at this time, the judgment rules: if \( y(jT_s + t_0) > v_0 \), then \( a_k \) is judged to 1; otherwise \( a_k \) is 0. It is clear that: only when the inter-symbol interference is very little, it can ensure the correct judgment of the above circuit. Thus, to reduce the bit error rate, a sort of communication IP core with encoding & decoding function should be designed.

3. Design of Base-band IP Core

A.. RTL Design of Base-band IP Core

As shown Fig. 4, the FPGA-based base-band IP core is built, by using the function modular idea. The entire process is presented below: Firstly, the task-scheduling module processes and analyses the control orders from PC, then, it activates the downlink-RF-encoding module, which will output PIE codes or set the command signals for RF circuit according to the command type. The uplink-echo-parsing module detects echo signal and notifies the data receiver when the frame is effective. At the same time, the frame is sent to the Miller-decoding module. The task-scheduling module converts the states according to the implementation state provided by the stat-judge module. When data processing of uplink and downlink is over, the result will be stored in the registers and sent to PC.

B. Design of IP Core’s sub-module

1) Data-transfer module: It includes series-parallel-converting sub-module, transfer-control sub-module and data-stored sub-module. The series-parallel-converting module achieves the parse of series protocol. The transfer-control sub-module can deal with the transmission’s logistic control according to the state machine, witch stores data in the data-stored sub-module.

2) Task-scheduling module: It is the processing corn of the whole design, whose internal state machine is divided into five states: receiving state, processing state, downlink-encoding state, uplink-decoding state and data-transmitting state. According to the implementation state of each sub-module, it converts the states of state machine to schedule the work of each module.

3) Downlink-RF-encoding module: It includes PIE-control sub-module and three sub-modules of modulation. The EPC-based PIE code is generated by the PIE-control sub-module. Through the modulation sub-modules, the digital codes are sent with clock pulse. The arbitrary rate of PIE signals can be achieved by adjusting the interval clock pulse.

4) Uplink-echo-parsing module: It includes synchronous echo processing, data receiving, frame detecting, Miller-decoding and decoding-control. It
detects the bus data, which will process the Miller codes when the frame is effective. The synchronous clock of echo processing is set 50MHz.

5) Clock-manage module: The steadily synchronous clock is achieved by the PLL of Quartus [6], and it can be divided into various clocks needed in the system.

6) Stat-judge module: It detects the implementation state of each module, providing the feedback information.

4. Simulation Study

A. Function simulation of IP Core

According to RTL design, through the serial data and Miller code input, the time wave and spectrum can be watched by the simulation tool of Quartus II. The wave of downlink PIE encoding is shown in Fig.4, wave of uplink echo Miller decoding is shown in Fig.5.

In Fig.5, en_ie_o is the enable signal of PIE, pie_clk is PIE synchronous clock, which is set to 80KHz, pie_code is the wave of PIE code, and other signals are the RF module’s configuration timing. sim_miller is the Miller code of simulation input, code_data_o is the data decoded, other is clock or enable signal.

B. Simulation of base-band transmission model

Simulation environment: By using Matlab7.2 and Simulink4.4, combined with the IP core, the single-step of simulation is set to 0.01, and the transmission channel is interfered by the AWGN noise which gradually changes from 0 dB to 60 dB.

Simulation process: By using Simulink tools of Matlab, the IP core is loaded into Matlab library. The PIE codes are modulated after the uplink-echo source module is built in the channel with AWGN noise. The Miller codes decoded by IP core will be compared with the original binary sequences to achieve the bit error rate.

In the simulation process, by changing the AWGN white noise, in the conditions of variational signal-to-noise ratio, the bit error rate of the simulation model is achieved, as shown in Fig.6.

5. Conclusions

In this paper, a base-band transmission model of RFID system is presented, and a sort of IP core based on the above model is designed. Through the function verification and simulation, the result shows that the above IP core has good accuracy and strong anti-interference capability. Compared with other design, the design of IP core has the advantages of easier maintenance and less hardware resources.

In accord with requirement of the practical applications based on EPC protocol, the above model and IP core provide an effective reference for the scientific and rational design of RFID system.

6. References